

Application No.: 09/752,122

Docket No.: JCLA6705

REMARKS**Present Status of the Application**

The abstract was objected by the Office Action. The Office Action further objected claim 6 under 37 CFR 1.75(c), and objected claims 1, 5, and 9-12 because of some informalities and rejected claims 1, 5, 9 and 12 under 35 USC 112. The Office Action rejected all pending claims 1-14 under 35 USC 103(a) as being unpatentable over Potash (US 4435756) in further view of Patterson and Hennessy, *Computer Organization & Design*, 2nd Ed., 1998 (hereinafter, Patterson). Applicant has amended the abstract and claims to overcome the objection and amended claims 1, 5, 9 and 12 to overcome the rejection under 35 USC 112. After entry of the foregoing amendments, claims 1-5 and 7-14 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of objections

According to the Office Action, the abstract was objected. In response thereto, applicants have amended the abstract to provide proper content of an abstract of the disclosure.

Further, claim 6 was objected under 37 CFR 1.75(c), and claims 1, 5, and 9-12 were objected to because of some informalities. In order to overcome the objections, claim 6 is deleted and claims 1, 5, and 9-12 are amended.

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Discussion of Office Action Rejections**[35 USC 112 Discussion]**

The Office Action rejected claims 1, 5, 9 and 12 under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term "a fetch instruction" is an instruction to be fetched from a memory location, and corresponding amendment is added into the claims to improve the clarity of these claims. After entering the amendment, claims 1, 5, 9 and 12 are believed to conform to 35 USC 112, second paragraph, and rejections under 35 USC 112 to these claims are respectfully requested to be withdrawn.

[35 USC 103 Discussion]

The Office Action rejected claims 1-14 under 35 USC 103(a) as being unpatentable over Potash in view of Patterson. Applicants respectfully traverse the rejections for at least the reasons set forth below.

Claim 1 is patentable over Potash in view of Patterson at least because combination of the two citations does not disclose, suggest or teach the feature of "...if the fetch instruction is not stored in the cache memory, the cache memory determines whether to fetch the fetch instruction from an external memory according to the control signal" as claimed in claim 1. More specifically, as stated in the Office Action, Potash has not taught to fetch the fetch instruction from an external memory according to a control signal if the instruction is not in the cache memory (page 6, point 12). Furthermore, Patterson taught a cache exists between the main memory and the processor, which operates in a manner such that when a fetch of data at an

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address results in a cache miss, the data is instead brought from memory into the cache and processor (p.541-2, p.545, 550). Accordingly, Patterson taught to *always fetch* the missed data from an external memory when a cache miss is occurred. Moreover, according to line 46, column 6 to line 7, column 5, Potash taught that no matter the branch instruction is success, subsequent instructions were always fetched. However, the present invention does not always fetch the missed data when a cache miss is occurred. Instead, the present invention determines whether to fetch the missed data according to a control signal as cited in claim 1. In other words, although a cache miss happened, the missed data may not be fetched from the external memory because the control signal prevented the cache from doing so.

Further, signal 64A in the Potash was not used to determine whether to access a memory. Potash discloses in line 65, column 7 to line 3, column 8 that “ ... In that case, write control circuit 63 operates to generate an encoding on leads 64A corresponding to a PT/LT state, and to send a write command over conductor 64B. That information is sent over bus 64 to the memory where it is written in the memory at the location specified by the address on conductors 64C.” Moreover, according to Figs. 4A-5B and corresponding description (line 40, column 4 to line 55, column 5), Potash used different coding in OP code of a branch instruction, and signal 64A is data to be written into the OP code. It is obvious that signal 64A is not a control signal as stated in the Office Action (page 6, lines 1-2).

Accordingly, Potash does not teach to send a control signal to the memory such that whether to perform memory access is determined, and moreover, combination of the two

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citations does not disclose, teach or suggest all features in claim 1. Claim 1 is therefore patentable over Potash in view of Patterson at least because the reasons set above.

Claims 5, 9 and 12 claims similar features as cited in claim 1, and therefore are patentable over Potash in view of Patterson at least because the reasons set above for claim 1.

Claims 2-4, 7-8, 10-11 and 13-14 are patentable over Potash in view of Patterson as a matter of law since the depended claims 1, 5, 9 and 12 are patentable over Potash in view of Patterson, respectively.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1, 5, 9 and 12 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-4, 7-8, 10-11 and 13-14 patently define over the prior art as well.

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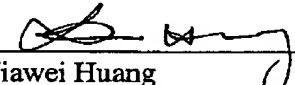
CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-5 and 7-14 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,
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